We claim:

1. A method of programming a radiation-hardened integrated circuit comprising:

supplying a prototype memory device to a customer;

receiving a final debugged customer-developed data pattern;

loading the customer-developed data pattern into memory;

programming the customer-developed data pattern from the memory into a number of pin-compatible production memory devices;

irradiating the production memory devices sufficiently to burn the data pattern into memory; and

shipping the irradiated and programmed parts to the customer.

2. The method of claim 1 in which programming the customer-developed data pattern comprises:

setting the gate voltage on at least a first N-channel memory transistor to ground; and

setting the gate voltage on at least a second N-channel memory transistor to VDD, wherein the first and second N-channel transistors define a complementary data state.

3. A method of converting a soft SRAM memory into a radiation hardened read-only memory, the method comprising:

programming a data pattern into an SRAM memory;

irradiating the SRAM memory at a total dosage of between 300K and 1 Meg RAD in order to burn the data pattern into memory.

4. The method of claim 3 further comprising shipping the irradiated and programmed parts to the customer.

5. A radiation-hardened SRAM memory cell comprising:

complementary column select lines;

a row select line;

cross-coupled first and second P-channel transistors;

cross-coupled first and second N-channel transistors, the current paths of the first P-channel and first N-channel transistors being coupled together at a first node and the current paths of the second P-channel and second N-channel transistors being coupled together at a second node;

a pair of pass transistors for transferring a complementary data state from the first and second nodes to the complementary column select lines,

wherein a gate of the first N-channel transistor is biased to ground and the gate of the second N-channel transistors is biased to VDD, the first and second N-channel transistors being irradiated to a sufficient dosage to establish a permanent data state in the memory cell.

6. A radiation-hardened memory cell as in claim 5 in which each of the pair of pass transistors comprise N-channel transistors.

7. A radiation-hardened memory cell as in claim 5 in which the first and second N-channel transistors have been exposed to a total dose or radiation between 300K and 1MEG RADs.

8. A method of using a radiation-hardened integrated circuit comprising:

receiving soft prototype memory devices;

developing a final, debugged, data pattern using the soft prototype memory devices;

shipping the final data pattern to the factory;

receiving irradiated pin-compatible production memory devices including a read-only version of the final data pattern from the factory.

9. The method of claim 8 in which receiving soft prototype memory devices comprises receiving prototype memory devices including at least one SRAM memory cell.

10. The method of claim 8 in which receiving irradiated pin-compatible production memory devices comprises receiving production memory devices including at least one SRAM memory cell.

11. The method of claim 8 in which receiving irradiated pin-compatible production memory devices comprises receiving production memory devices that have been exposed to a total dose radiation of at least 300K Rads.

12. A radiation-hardened SRAM memory cell comprising:

first and second nodes;

first and second transistors having current paths coupled at the first node, and gates coupled to the second node;

third and fourth transistors having current paths connected at the second node, and gates coupled to the first node, wherein

the second and fourth transistors being irradiated with a sufficient dosage to induce a permanent complimentary data state at the first and second nodes.

13. The memory cell of claim 12 in which the second and fourth transistors each comprise N-channel transistors.

14. The memory cell of claim 12 in which the first and third transistors each comprise P-channel transistors.

15. The memory cell of claim 12 in which the gate of the second transistor is set to a logic one voltage and the gate of the fourth transistor is set to a logic zero voltage prior to irradiation.

16. The memory cell of claim 15 in which the logic one voltage is about 2.7 volts and the logic zero voltage is about zero volts.

17. The memory cell of claim 12 further comprising:

a pair of complementary column select lines;

means for coupling the complementary column select lines to the first and second nodes; and

a row select line coupled to the coupling means.

18. The memory cell of claim 17 in which the coupling means comprises first and second pass transistors.

19. The memory cell of claim 18 in which the first pass transistor comprises an N-channel transistor having a gate coupled to the row select line.

20. The memory cell of claim 18 in which the second pass transistor comprises an N-channel transistor having a gate coupled to the row select line.

21. A programmable key method comprising:

providing a plurality of key circuits;

writing a data pattern into a plurality of key circuits; and

irradiating the key circuits at a total dosage of between 300K and 1 Meg RAD in order to burn the data pattern into memory.

22. The method of claim 21 in which providing a plurality of key circuits comprises providing a plurality of circuits each including an N-channel transistor and a resistor coupled together in a source-follower amplifier configuration.

23. The method of claim 21 in which providing a plurality of key circuits comprises providing a plurality of circuits each including an N-channel transistor and a resistor coupled together in a common-source amplifier configuration.

24. The method of claim 21 in which providing a plurality of key circuits comprises providing a plurality of circuits each including an N-channel transistor and a P-channel transistor coupled together in a common-source amplifier configuration.